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Abstract

In this paper, we present a short overview of the power dies interconnects based on PCB technology, then we focus on embedding of power dies in the PCB material. In the second part of the article, we present in details the technology we developed to embed dies in PCB. Results show that the electrical performance of the die remains satisfying after embedding, but that dies with a copper topside metal layer are required for this process.

Keywords

3-D packaging, PCB, DBC

1 Introduction

Current and future power semiconductor devices (especially those based on silicon carbide – SiC – or gallium nitride – GaN –) offer very high switching speed capability. Current fast transistor can switch currents of several kiloamperes per microsecond, and voltages of more than 10 kilovolts per microsecond. This makes it possible to increase the conversion efficiency (shorter switching transient, hence lower switching losses), or to reduce the size of the converters (by increasing their switching frequency and using smaller passive components). To take full advantage of these fast devices, it is, however, necessary to design very-low inductance interconnects. For example, in [1], the authors present a switching cell with a sub-nanohenry stray inductance designed for GaN transistors. They also integrate the gate-drive circuit to supply fast control signals to the transistors. For such high-density interconnects, the printed-circuit board (PCB) technology is very attractive. Another clear trend in power electronics is the increase in power density. As a consequence, and despite the improvement in conversion efficiency, the active devices dissipate a lot of heat (100 to 300 W/cm²). Therefore, they must be attached to a low-thermal resistance cooling system. Classically, ceramic substrates (especially DBC, for Direct Bonded Copper) are used [2]. In this paper, we focus on packaging solutions where active dies are attached on a DBC substrate (for thermal management), and then embedded in layers of PCB. We start by presenting a review of the existing solutions from the literature, and then we present some prototypes we assembled in the lab.

2 Review of PCB-based Die interconnects and of Die Embedding in PCB

Although it can be found virtually everywhere, the "standard" power electronics interconnection technique (wirebonding) has many drawbacks: as discussed above, it generates relatively large stray inductances (several nanohenries); it occupies a non-negligible area on the substrate (all the interconnections are performed on the same plane); it is time-consuming to manufacture (all wirebonds must be placed successively).

As a consequence, many researcher have tried to overcome these limitations. Among the various solutions proposed, we will focus on those that make use of flexible or rigid PCB technology. Indeed, this technology is very mature, offers a variety of interconnect possibilities, and makes it possible to process many dies at once.

One first solution to make converters more compact is

based on the flex PCBs: once they are populated with the components (in standard Surface-Mount Technology, SMT), they can be rolled around the larger component [3] or folded in a sophisticated fashion [4]. Such approach may make thermal management difficult, and seems more suited to low-power converters (up to a few hundred watts).

Another use of the flex PCB is as direct replacement for the wirebonds: the power semiconductor dies are attached to a DBC substrate, and a flex PCB is attached on top of the devices. This flex PCB also provides the interconnections between the topside of the dies and the DBC substrate if needed. Such solution requires dies with a suitable topside metal [5] (most power dies have an aluminium layer, which is suited to wirebonding, but not to soldering or sintering). Compared to wirebonds, the flex PCB offers higher interconnect density [6], especially because it can have several layers. Furthermore, auxiliary components (such as the gate drivers) can be mounted directly on the flex PCB [7]. Commercial power modules that use flex PCB instead of wirebonds are available from Semikron [8].

Another set of solutions is based on rigid PCBs rather than flex. Rigid PCBs are thicker (from a few hundred of microns up to a few millimeters), so it is possible to integrate devices inside the PCB. For example, various manufacturers sell dielectric layers that can be stacked in a multilayer PCB to form capacitors [9]. An example of a converter integrating such capacitive layers is given in [10]. In this paper, the authors also embed some magnetic layers to form an "embedded Passive Integrated Circuit" (emPIC).

However, most papers focus on integrating the active rather than the passive devices in the PCB. This allows for a shorter distance between the active die and the cooling system. PCBs have poor thermal conductivity (usually lower than 1 W/m.K, as compared to 24 W/m.K for alumina or 150 W/m.K for AlN ceramics), and power semiconductor devices have a high power density to dissipate (100 W/cm^2 or more).

Some authors do not use the PCB material, but the structure they propose offer many features of PCB-embedding. For example, in [11], power dies are attached on a DBC and integrated in a ceramic frame. In [12], a polyimide (Kapton) layer is used around the dies. Finally, the "SiPLIT" technology [13], uses some steps of the PCB technology (lamination, electroplating) to form a power module with very low parasitic inductances.

A list of commercially-available, PCB integration technologies for active devices (not limited to power devices) is given in [14]. Many of these technologies were developed through the European projects "Hermes" and "Hiding Dies", or through the German project "HiLevel". These projects included work on the manufacturing technology, on the design tools, and on validation [15].

In particular, one of the demonstrators of the "HiLevel" project included a 50 kW inverter for hybrid cars. It is described in [16]: the dies are attached to a thick copper layer (no DBC used here), and then embedded in PCB laminates. The pads of the dies are then exposed by removing some of the PCB material with a laser.

In [17], the exposition of the pads is performed by mechanically grinding away some of the PCB materials. The resulting converter offers very low parasitic inductances, and allows for very close decoupling, as the decoupling capacitors are mounted directly on top of the power semiconductor dies.

Other technologies use a "face down" approach, where the dies are first attached in a "flip-chip" orientation to a patterned copper foil. This seems more suited to high-density chips such as microprocessors [18].

3 Proposed Embedding Technique

3.1 Overview of the process

The process flow of the proposed embedding technique is visible in figure 1.

The dies are first attached to a patterned DBC substrate using silver sintering (fig 1a). This technology offers high electrical and thermal performance, and can sustain the remaining manufacturing steps. As it is a solid-state process, there is no movement of the dies during sintering (as opposed to soldering, where dies usually move slightly during reflow). This is very important, as a good positioning accuracy (in the order of 100 μm for power devices) is required later to contact the topside of the dies.

Then, we stack a set of pre-impregnated sheets of glass fibre (with the shape of the dies cut-out) on top of the DBC/die assembly, plus a sheet of copper (fig. 1b). This stack is then laminated under pressure, using the standard PCB manufacturing technology (fig. 1c). The copper layer is open above the dies (using standard PCB lithography and wet-etching) (fig. 1d). A CO_2 laser is used to ablate the glass fiber/resin composite exposed through the windows in the copper layer (fig. 1e). It is worth noting that although it is relatively thin (3 μm) the topside metal of the devices is not damaged by the laser. Finally, an electroplating process (identical to the process used for PCB through-hole plating) allows to connect the topside pads of the embedded dies with the top copper layer (fig. 1f. From this step, the resulting assembly can be used as a standard PCB, allowing to pattern the copper layer, to add more layers (for higher circuit complexity), and to attach surface-mount components (passives, gate drivers, etc.)

In the following sections, we give some more practical details on this process

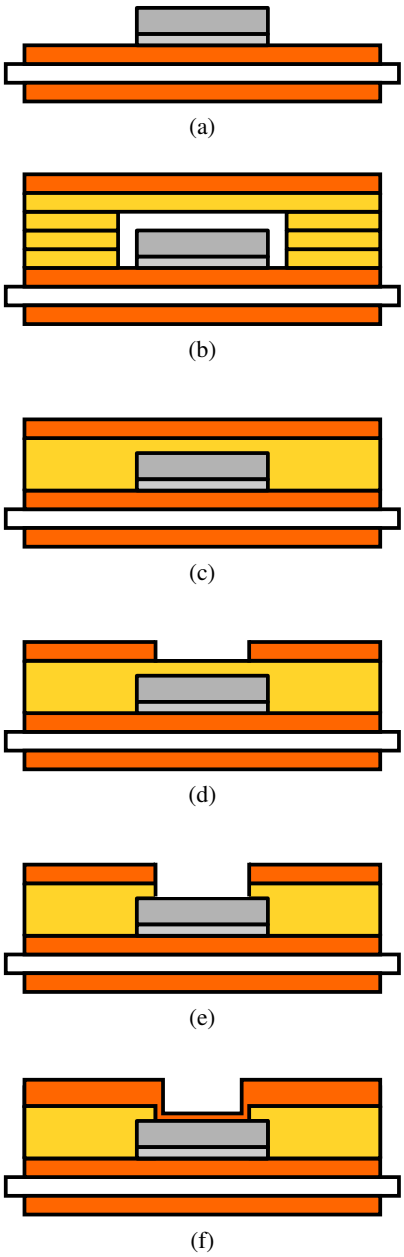

Figure 1: Die embedding technique proposed in this paper: (a) a die is attached to a DBC substrate. Layers of laser-cut prepreg foils are then stacked around the die (b) with a copper foil on top, and laminated (c). Windows are etched in the copper layer (d), and used as a mask for the laser-ablation of the PCB material (e). Finally, copper is electroplated on the top surface (f).

3.2 Preparation and mounting of the dies

The dies used in this paper are 1200 V, silicon diodes with a die size of 9×9 mm^2. They have a standard backside silver finish, and a topside aluminium metallization (required for aluminium wirebonds). Some of the diodes received layers of Ti/Cu (deposited by PVD through a polyimide mask, with thicknesses of 50/150 nm, in an EVA300 system) on their topside.

The diodes were then mounted on bare copper substrates using the following pressure-less silver-sintering process:

- screen printing of Heraeus LTS 117O2P2 silver paste (thickness 50 μm). The printed pattern consists in 16 smaller squares with a 300 μm spacing between them to form the 9×9 mm^2 footprint. This is used to achieve better drying of the paste despite the large surface area of the dies;
- placement of the die on top of the fresh paste deposit using a JPF Microtechnic PPOne die bonder (for proper alignment and control of the force applied on the die, around 0.1 N);
- drying of the paste, 85 °C for 30 min;
- sintering stage: fast ramp-up (70 °C/min) up to 240 °C, and 30 min maintained at 240 °C.
- natural cooling down

The process takes place in air, causing the bare copper substrates to oxidize, but this was not an issue for the following steps.

3.3 PCB embedding

Two reference of prepreg sheets are used for the PCB embedding: Isola PCL 370HR (high Tg FR4 material) and Arlon 55NT (non-woven epoxy-aramide material).

The FR4 material is used in the stacking to match the die thickness, and a cutout slightly larger than the diode is performed in the sheets of prepreg (fig. 1b). 3 layers of prepreg are stacked.

The non-woven material is used as the topmost layer, the one that covers the diode (fig. 1b). It is used because the laser ablation which comes later in the process leaves fewer residues on the surface of the die. It is, however, a more expensive material than FR4, which is why it was not used for the whole prepreg stack. Finally, a sheet of copper (35 μm) is added to the stack prior to lamination, which is performed under 13 bars and 195 °C for 90 minutes in an LPKF Multipress S laminator.

After lamination, the topside copper layer is etched away to open a window corresponding to the pads of the

embedded die (fig. 1d). This step requires proper alignment with the die, but this remain less demanding than any High-Density Interconnect (HDI) multi-layer PCB, a technology which is commonplace nowadays [18]. A positioning accuracy of 100 μm is sufficient to match the smallest pad size of a power die (typically the gate contact on a MOSFET or an IGBT, which is designed to be connected with a 100-125 μm wedge wirebond.

Laser ablation of the laminate material is performed on a Gravograph LS100EX 60 watt CO_2 laser (10.6 μm wavelength). Preliminary tests showed that the parameters of the laser (namely sweep speed and power of the beam) had little influence on the quality of the result, providing the beam is slow enough or powerful enough to remove the organic material. In all cases, we did not observe any change in the appearance of the topside metal of the dies. This is very interesting, as it demonstrates a very good selectivity of the laser ablation: it easily removes the laminate, but stops completely once it reaches the die. Another advantage of this good selectivity is that we can use the laminated copper layer as a mask for the laser ablation process: there is no need for accurate alignment of the laser with the chips; a coarse positioning is sufficient, providing the laser sweeps an area larger than the openings in the copper layer.

As the ablation is performed in air, cleaning in isopropanol is required to remove some residues. A protective atmosphere (N_2) should help reducing these residues.

The last step of the embedding process is the electroplating of a copper layer over the entire surface of the PCB, including the die cutouts (fig. 1f). We use the standard "plated-through-hole" process (Bungard).

Once this process is over, the resulting DBC/PCB can be handled like a standard PCB: etching of a pattern in the topside copper, lamination of more layers, reflow soldering of SMT components, etc. The only restriction applies to the drilling of vias: only blind vias are allowed, as the ceramic material of the DBC is too hard for the drill bits.

4 Results

4.1 process parameters

Two sets of dies were processed as described in fig. 1: the first set was used as supplied, while the second set received a PVD plating (Ti/Cu) over its aluminium topside metallization.

The surface roughness of the metal on top of the dies was measured using a stylus profilometer (Tencor), and some of the results are presented in figure 2. The blue line (top) corresponds to a measurement performed on the Al metallization before any treatment. The green line (middle) is the surface profile of an embedded die which received a Ti/Cu plating and the red plot (bottom) is the surface profile of an embedded die without Ti/Cu plating (the electroplating process was performed directly on the Al topside metal of the diode).

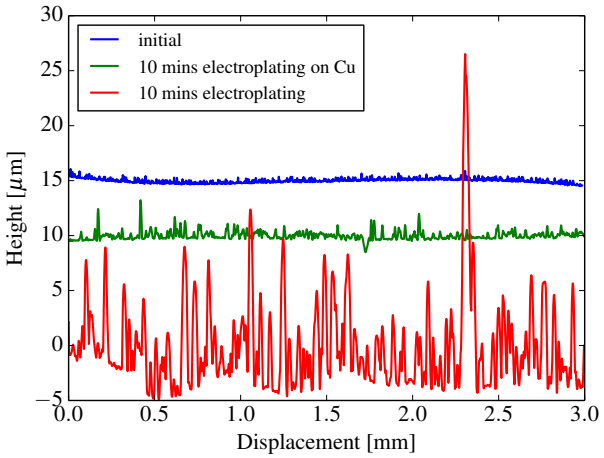

Figure 2: Surface roughness (stylus profilometer measurement) of a die before processing (initial), and after processing. The die that received a PVD plating of Ti/Cu before embedding shows a much lower roughness than the die that was directly embedded (with standard Al topside metal). The plots are shifted vertically for better clarity.

While both the green and red plots show an increase in roughness compared to the initial measurement (blue), this increase is moderate in the case of the die that received a Ti/Cu plating prior to the electroplating process. This is especially true when considering the thickness of the copper layer (3–10 μm) which is electroplated. In the case of the direct electroplating on aluminium, however, the surface roughness is much worse, with a peak of up to 25 μm. This confirms the visual aspect of the dies after electroplating: in the case of the Al dies, the electroplated copper is dull, while it is shiny in the case of the dies which received a Ti/Cu plating.

As a consequence, and despite it requires an extra processing step, a Ti/Cu plating of the dies seems necessary to improve the quality of the topside contact in our embedding process. This is in agreement with some of the processes described in the introduction, which require copper-finished dies. These are becoming more common nowadays, because of the development of copper wirebonds [19], but they remain a minority compared to aluminium-finished dies.

4.2 Electrical characterization

The static characterization of an embedded diode is presented in figures 5 and 6. The forward characteristic was measured using a Tektronix 371A high power curve tracer, with 4-points connections to the PCB substrate. The series resistance of this diode (slope of the linear part

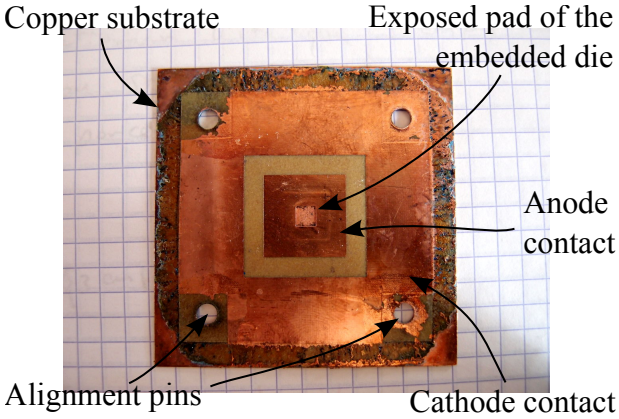

Figure 3: Sample used for electrical characterization (60×60 mm^2). A diode with an aluminium topside metal was used, which explains the dull aspect of the electroplated copper on the exposed pad.

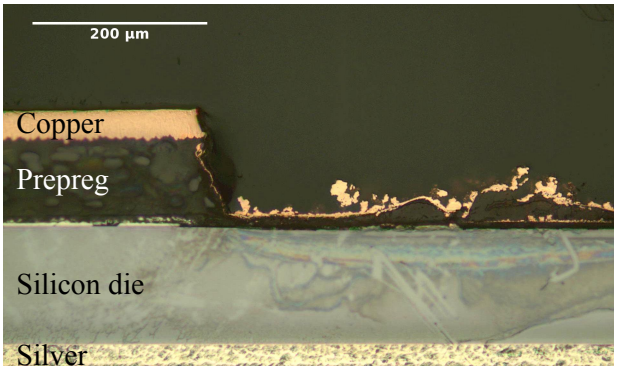

Figure 4: Cross-section of the sample pictured in figure 3, taken at the edge of the exposed pad. The poor quality of the copper electroplated on the die is clearly visible.

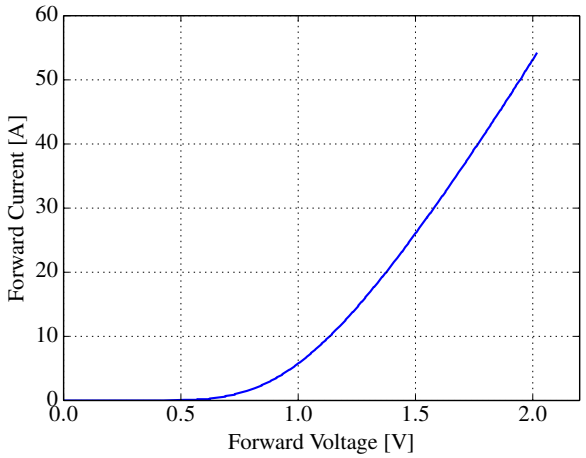

Figure 5: Forward characteristic of the embedded die

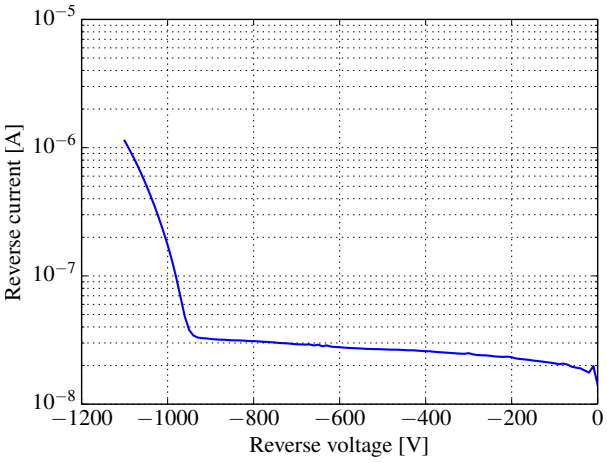

Figure 6: Reverse characteristic of the embedded die

of fig. 5) is high. This is due to the poor quality and low thickness of the electroplated copper layer (see fig. 4).

The reverse characteristic (figure 6) was measured using a Keithley 2410 high-voltage SMU up to 1100V (limited by the equipment. A second measurement was performed using the Tektronix 371A in high voltage mode. This second measurement is much less accurate, but indicates that the breakdown voltage of this embedded die occurs at around 1350 V. This shows that no arcing was detected, and that the embedding of the die constitutes a satisfying encapsulation. Further work is required to assess this encapsulation, especially in presence of moisture or after thermal cycling.

5 Conclusion and Perspectives

Embedding of dies in PCB material is a promising technology, It allows for more compact systems, makes it possible to process many dies at once, and offers superior electrical performance compared to wirebonding. The thermal performance of PCB, however, is often not sufficient for power electronics applications above a few tens or hundreds of watts.

Therefore, a solution is to use a substrate such as DBC for the thermal management, and to laminate PCB layers on top, for the electrical interconnects. This was already presented in the literature, by several research groups (section 2). However, most of the results that can be found (from companies and organizations such as AT&S, Schweizer, Fraunhofer IZM) rely on advanced equipment designed for large scale manufacturing of PCBs. Such equipment can only be afforded by a few research groups.

Here, we presented in details the embedding process we developed, based on prototyping-scale PCB equipment. Although not as accurate as the state of the art machines for PCB manufacturing, this allows for low cost evaluation of the embedding technology.

A simple demonstrator is presented in the paper (a diode attached on a copper substrate using silver sintering, and embedded in PCB). Electrical characterizations show satisfying forward and reverse characteristic of the packaged die.

The current work is focused on embedding several dies at once (diodes and transistors), to form a complete switching cell (including DC capacitors). This is necessary for the characterization of the dynamic behaviour of the packaging.

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